What is Claimed is:

1. A dynamic power management device for supplying power to a solid state memory integrated circuit, said device comprising:

power control means for supplying a variable voltage to said memory integrated circuit; and

logic control means responsive to data access activity for generating address and control signals for said memory integrated circuit and for controlling said power control means to supply power to said memory integrated circuit sufficient to maintain memory information in said memory integrated circuit during periods of no data access activity and sufficient to exchange memory information with said memory integrated circuit during periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

2. The apparatus of Claim 1, further comprising I/O means for converting parallel data signals to serial data signals for input to said memory integrated circuit and for converting data signals output from said memory integrated circuit from serial to parallel and performing error correction on the resulting parallel data signals.

3. The apparatus of Claim 2 wherein said power control means comprises means for selecting between alternate power sources, a switching regulator, and means for feeding voltage information back to said logic control means.

4. The apparatus of Claim 3 wherein said voltage information includes both voltage output information used by said logic control means to cause said power control means to maintain a specified voltage output, and voltage source information used by said logic control means to cause said means for selecting to select one of said alternate power sources.

5. The apparatus of Claim 2 wherein said logic means comprises a DMA controller, a data sequencer, and a timing sequencer.

6. The apparatus of Claim 5 wherein said logic control means further comprises refresh timer means for timing refresh intervals, a binary address generator, and an encoder, together for generating said address signals for said memory integrated circuit.

7. The apparatus of Claim 2 further comprising slew rate controller means for limiting the time rate of change of

voltage of said control signals and said data signals input to said memory integrated circuit.

8. The apparatus of Claim 2 wherein said logic control means causes said power control means to supply to said memory integrated circuit a relatively low voltage during a standby period, a higher voltage during memory refresh, and a still higher voltage during memory access.

9. The apparatus of Claim 2 further comprising daisy chain controller means for enabling communication with another dynamic power management device.

10. The apparatus of Claim 2 wherein said logic control means is provided with a sleep mode for conserving power during periods of inactivity.